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A Low Power down Conversion CMOS Gilbert Mixer for Wireless Communications

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Abstract
In this paper a design of low power 2.4GHz (RF) down conversion Gilbert Cell mixer, implemented in 0.18µm CMOS technology with 1.8V supply voltage is presented. The obtained result shows a conversion gain equal to 6.7dB and third order Input intercept point -1db, power consumption of 3.86mW at 1.8V supply voltage. The 50Ω matched impedance condition is applicable. Result shows a good potential of this CMOS mixer and justify its use for low-power wireless communications.
Keywords—Mixer, Gilbert Cell, RFIC, CMOS Technology, linearity, down conversion

I. Introduction

Mixer is non linear and time variant device. RF mixer plays an important role in a communication receiver. It translates RF frequency to IF frequency by using LO(local oscillator). Conversion process in time domain is performed by multiplying the RF signal by a signal named Local (LO).Nonlinearity effect of the mixer is necessary for this frequency translation in order to produce sum and difference frequencies. Nowadays, with the development of the wireless communication technology devices, demand for the wireless service has been constantly increasing. Therefore, 2.4GHz is the frequency band which is set free for the industrial,but today bipolar transistor replaced by cmos because it consume less power, high performance and high speed. The RF receiver consist of LNA, Mixer and filter, among these the mixer decided the overall performance of the receiver.

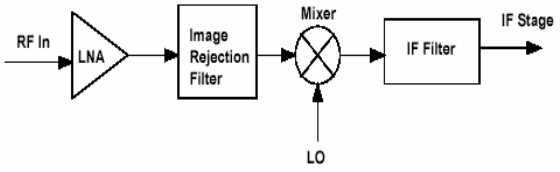

Fig.1 Down Converter Mixer as a Multiplier in Receivers

A high linearity and gain is very important parameter to overall performance of mixer. In this paper a design of Gilbert mixer in 0.18 µm process technology to improved linearity and gain as compared to the conventional mixer is shown.

II. Qualitative Description of Proposed Mixer

Mixer design consists of three SCP's(source coupled pair stage). In first stage, The transistor M_1,M_2 is a input trans-conductance stage which convert the RF input signal to current signal on the other hand, the transistor M_3, M_4, M_5 and M_6 are called switching stage in which LO signal mix with tail current to produce IF(intermediate signal), performance of the mixer can be improved by using, biased voltage for RF signal. Current biasing circuit can be replaced by MOS transistor, by which linearity is improved. The third order intercept point and the conversion gain of the mixer is a given by the equation given below.

$$Gc = \frac{2}{\pi gmRL} = \frac{2}{\pi R}\left(\frac{\mu nCoxW}{L\ Id}\right)^{1/2}$$

$$IIP3 = \frac{8\ VsatL}{3\mu 1Rs} Vod\left(1+\frac{\mu 1Vod}{4VsatL}\right)\left(1+\frac{\mu 1Vod}{2VsatL}\right)^2$$

III. GILBERT MIXER DESIGN

Lots of methods have been proposed to improve the linearity of the mixer due to the nonlinear phenomenon of the transconductance stage. Using source degeneration connected to the sources of the transconductance stage in a Gilbert cell mixer is commonly published [1,2]. Trade-offs between the conversion gain and the linearity are con-sidered by designers while using the method described previously. Another way to enhance the linearity of a mixer, is based on CMOS gm Cell composed of the tanh functions [3,4] . As charge-injection method employs current injecting into the drain of the transistors in the transconductance stage, it increases the current in the transconductance stage and is proportional to the value of IIP3 and the conversion

gain [5] . But the improvement in the aspect of 1IP3 is not much. Hence, A method to improve the linearity is to use a modified Class-AB high-linearity Transcooductance [6].

A Gilbert cell is shown in fig.2 it is often used structure in down conversion mixer. This cell involves two part input stage and switch stage, input stage generally called trans-conductance stage which consists of M_1, M_2 which converts RF voltage signal to current signal. The switch stage consist of M_3, M_4, M_5 and M_6 which driven by LO signal. Transistor M_3 M_5 and M_4 M_6 turn on alternately in positive half period, that means LO signal must be kept a suitable magnitude to ensure switching accurately. Linearity is mainly decided by trans-conductance stage. In this work, we replace bipolar to CMOS transistor.

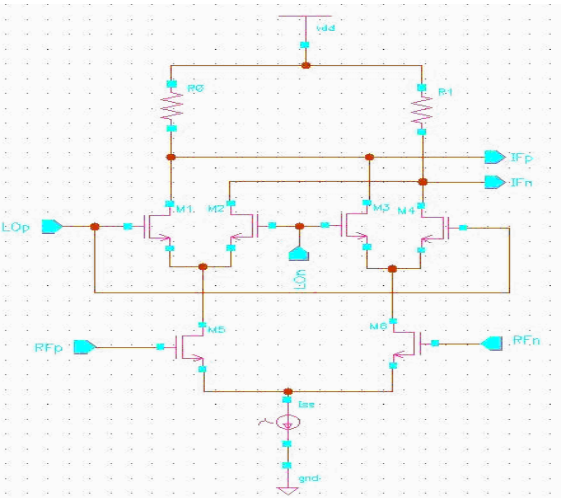

Fig.2 Gilbert Mixer

As the saturation region offers higher gain and makes the current less susceptible to the changing voltage across the transistors, almost all the transistors are designed to operate in this region [3]. The gain stage transistors should be biased such that they have enough head room to swing without leaving the saturation region, therefore the over drive voltage (Vgs-Vt) should be assumed around 200mV to 400mV. The local voltage level should be large enough to make the conversion gain insensitive to the LO amplitude. But if *LO* becomes too large, it reduces the switching speed and increases the LO feed through, thus for complete switching, *LO* should be between 100mV to 400mV. If two switching pair transistors conduct at the same time, noise increases. Therefore the overdrive voltage for switching pairs should be as close to zero as possible. Fig.3 illustrates the proper local switching [3].

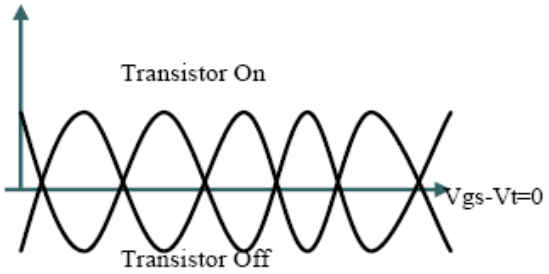

Fig.3 Proper local switching

To choose the appropriate architecture for any mixer, the system requirements are of the first priority. In the present study, the required mixer design specifications are as given below in table1.1

Parameter	**Value**
RF Frequency (GHz)	2.4
LO Frequency (GHz)	2.25
Conversion Gain (dB)	6.7
1-dB Compression point (dBm)	-1
Power Consumption (mW)	100
Noise Figure (dB)	15

Table1.1

Assuming that RL is the input impedance of the IF filter (300Ω -500Ω) and G_c is about 6.7dB, gm can be calculated using the equation (3).

$$gm = \sqrt{2knW.Id}/\mathrm{L}$$

IV. SIMULATION RESULT

The proposed Gilbert Mixer is designed and simulated in TSMC O.18µm RF CMOS process Using Cadence tool for high CG, low NF and reasonable IIP_3, a large DC current is required through the input gm stage only. Then a large load resistor (RL) in switching stage also gives higher CG and lower NF. Very low DC current through the switching transistors reduces DC offset, thermal noise and 1/f.

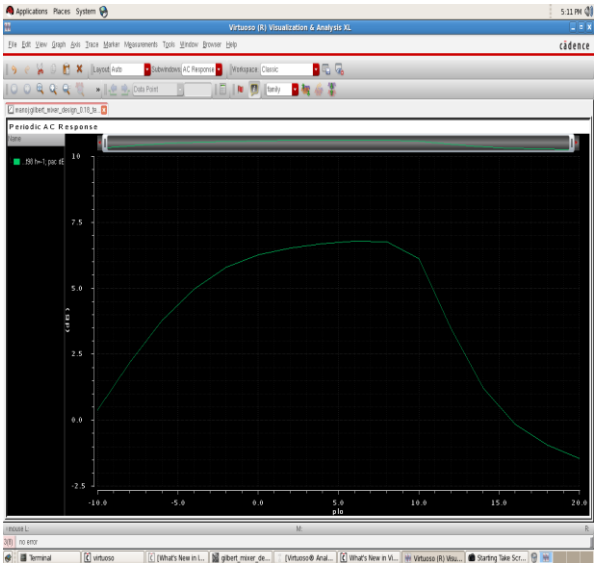

Fig4. Frequency response of conversion gain

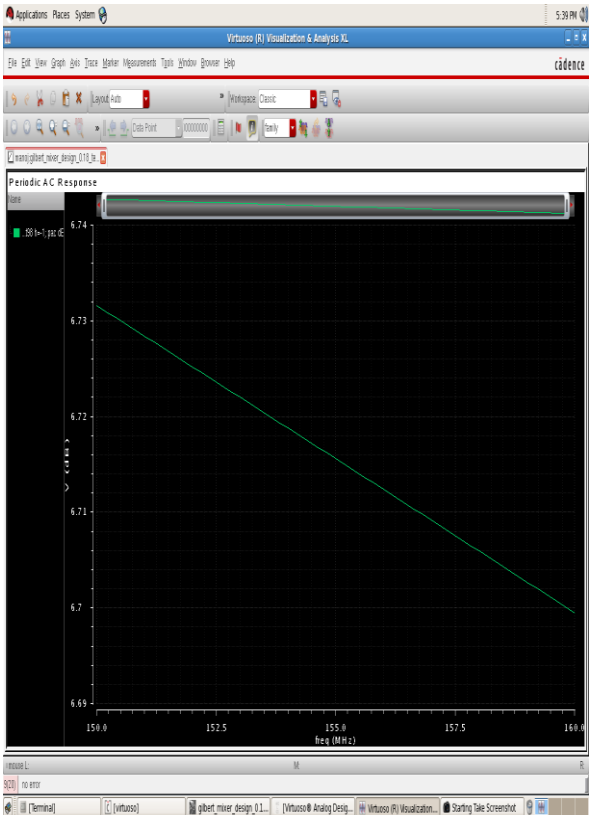

Fig5. Frequency response of

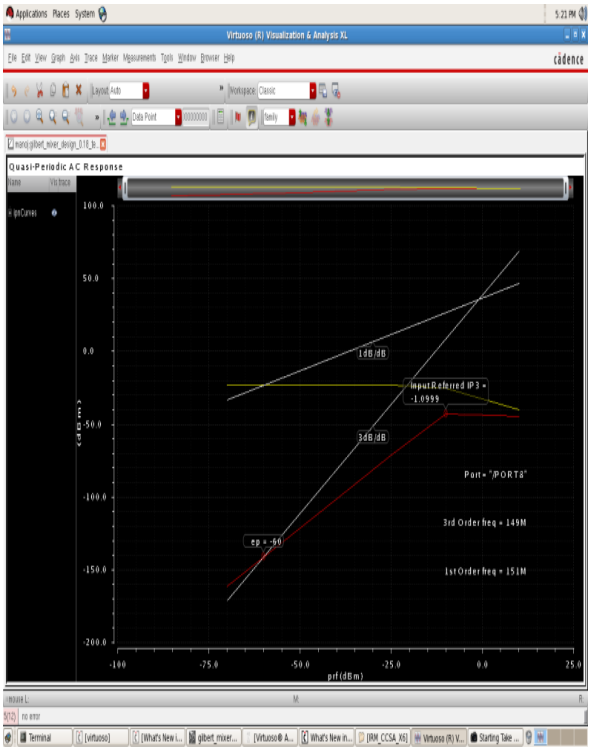

Fig6. Frequency response of IIP3

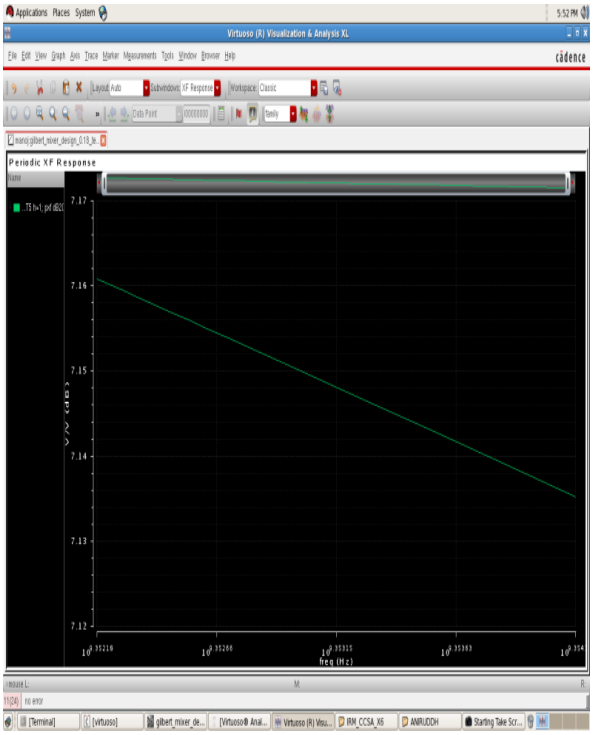

Fig7. Frequency response of conversion gain

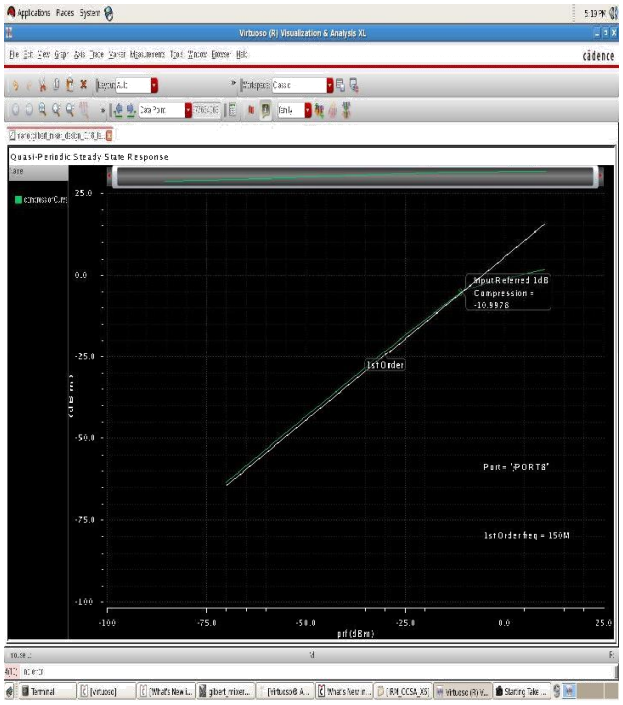

Fig8. Frequency response of 1dB compression point

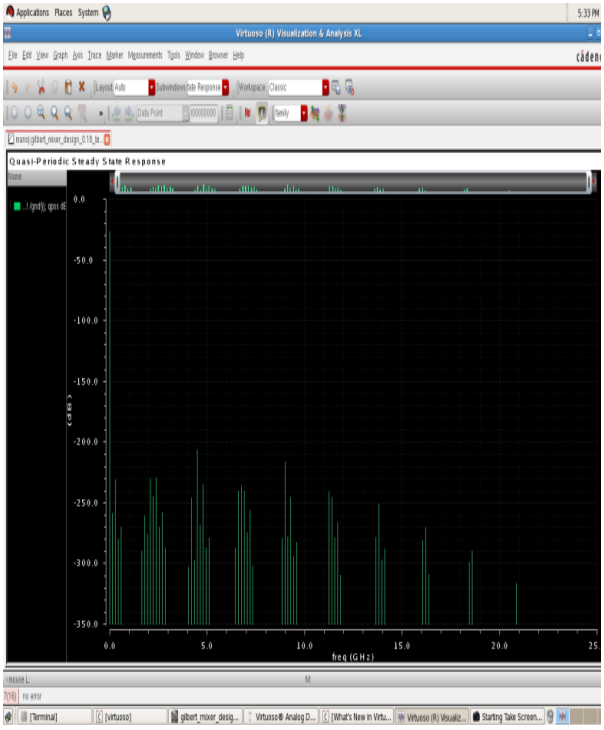

Fig9.Frequency response of Power consumption

V. Parameter comparison with conventional Mixer

Ref	Supply Volts	Freq. RF CG-(dB)	CG dB	IIP3 dBm	P-1dB dBm	Tech (um)	Power (mW)
1	2	0.9	1.1	-3.3	-15.4	0.35	7.2
2	1.8	1.9	7	-5	-10	0.18	3.8
3	1.5	2.4	3.3	5.46	-8.98	0.18	5.6
This work	1.8	2.4	6.78	-1	-10	0.18	10.0

VI. CONCLUSION

This paper demonstrates that a low-power, high performance UWB down-conversion mixer can be realized using O.18µm CMOS technology under 1.8V supply, gain is 6.7dB, IIP_3 and P_1dB are 1dBm and -10dBm. Charge injection method was used to increase the linearity and conversion gain of the mixer. This topology allows the designer to easily adjust the bias current of the input transistors while maintaining the bias currents in other parts of the circuit. This technique also reduces the Noise .The second technique which was used to increase the RF and LO isolation is the cascade devices method which caused a higher port to port isolation. As the active loads are also used to increase the conversion gain of the mixer, in order to have the output impedance matched, two source follower circuits were added to the designed system. As the simulation results illustrated the total system performance and accuracy, these techniques caused a better performance for the Gilbert Cell mixer in terms of the linearity, conversion gain, due to the importance of the mixers in the receivers, in this paper, a low voltage and low power fully integrated double balanced Gilbert cell mixer was designed and simulated using a 0.18µm CMOS process to achieve specific aspects and predefined working condition.

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AUTOBIOGRAPHY

Manoj Kumar Pandram has completed the B.E. degree in Electronics and Communication Engineering from R.E.C. Rewa affiliated to R.G.P.V Bhopal, India in 2010. He is currently pursuing M.Tech degree in Microelectronics and VLSI Design from S.G.S.I.T.S. Indore

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